IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Date: 17 December 2003

Robert B. Davies

Art Unit: 2815

Serial No.: 09/920,222

Filed: 01 August 2001 Examiner: Lee, Eugene

For: SEMICONDUCTOR DEVICE WITH INDUCTIVE COMPONENT AND METHOD OF MAKING

BRIEF FOR APPELLANT

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

Please consider the contents of the following Brief for Appellant.

I. REAL PARTY IN INTEREST

All of the right, title and interest in and to the above-described Patent Application are owned by appellant.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences related to the above described Patent Application.

III. STATUS OF THE CLAIMS

1. A copy of claims 1-7, 28-33, and 37-51, all of the claims in the application, is provided in Appendix A.

2. Claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 stand rejected under 35 U.S.C. 102(b), as being anticipated by Kendall, U. S. Patent No. 3,881,244.

3. Claims 4, 41, and 51 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Matsuzaki, Japan, 06-120036 A.

4. Claims 28 through 33 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Matsuzaki, Japan, 06-120036 A, in view of Kendall, U. S. Patent No. 3,881,244.

5. Claims 39, 40, 47, 48, and 50 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244.

6. Claims 44 and 46 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Farooq et al., U. S. Patent No. 6,574,859 B2.

IV. STATUS OF AMENDMENTS FILED SUBSEQUENT TO FINAL REJECTION

Claim 47 was amended after final rejection so that it depends from claim 46, rather than claim 45, to rectify an antecedent basis. This amendment has been entered, according to an Advisory Action mailed 15 October 2003.

V. EXPLANATION OF THE INVENTION

The application on appeal discloses and claims an integrated circuit 10, best seen in FIG. 10, and a method of fabrication, described in conjunction with FIGS. 1-9.

Integrated circuit 10 includes a low resistivity semiconductor substrate 11 with a dielectric region 14, including dielectric material 17 and cavities 16 closed by cap layer 38, formed therein (See FIGS. 1-3). A trench 40 is formed in dielectric region 14 with dielectric sidewalls (See FIG. 4). The lower surface of trench 40 is covered with a conductive material 51 that serves to conduct plating current I_{P1} equally across trench 40 (See FIGS. 5 and 6). An electroplated conductive material 47 is disposed in trench 40 by electroplating to produce an inductance (e.g. inductor 50 in FIG. 11), with the sides of the inductance bounded by the dielectric sidewalls and with the bottom of the inductance adjacent a cavity 76 (See FIG. 7). Adjacent cavity 76 is formed by isotropically etching the rear surface 34 of substrate 11, twice, and mounting integrated circuit 10 on a pedestal 74 of a die attach pad 72 (See FIG. 10). An active region 12 is formed adjacent dielectric region 14 and includes at least one active element, such as transistor 20.

VI. ISSUES FOR REVIEW

The first issue is whether claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 are anticipated by Kendall, U. S. Patent No. 3,881,244.

The second issue is whether claims 4, 41, and 51 are patentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Matsuzaki, Japan, 06-120036 A.

The third issue is whether claims 28 through 33 are patentable over Matsuzaki, Japan, 06-120036 A, in view of Kendall, U. S. Patent No. 3,881,244.

The fourth issue is whether claims 39, 40, 47, 48, and 50 are patentable over Kendall, U. S. Patent No. 3,881,244.

The fifth issue is whether claims 44 and 46 are patentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Farooq et al., U.S. Patent No. 6,574,859 B2.

VII. GROUPING OF CLAIMS

Appellant believes that grouping the claims by independent claims (1, 28, 37, 45, and 49) and claims dependent thereon might be easier to understand, since each of the independent claims includes different structure. However, appellant is willing to group the claims, as grouped by the Examiner, and has argued them accordingly.

VIII. ARGUMENT

Issue #1

Claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 are rejected under 35 U.S.C. 102(b), as being anticipated by Kendall, U. S. Patent No. 3,881,244. Appellant respectfully traverses this rejection.

The independent claims in this group are claims 1, 37, 45, and 49.

Claim 1 specifies "a trench defined in the dielectric region and including dielectric sidewalls, and an adjacent cavity defined at least partially by the substrate". Claim 1 further specifies an inductance with "the sides of the inductance being bounded by the dielectric sidewalls and the cavity being adjacent the bottom." It is clear from the claim language that the sides of the inductance are bounded by the dielectric sidewalls. It is also clear from the language that there is a cavity, defined at least partially by the substrate, adjacent the bottom of the inductance.

Turning to the disclosure of Kendall, it can immediately be seen that a solid state conductor is disclosed (note Kendall's title) and not an integrated circuit, as disclosed and claimed by appellant. The present invention includes a flat inductor formed in a trench, which means it is basically a two-dimensional structure, ignoring the depth of the electroplated material in the trench (for example, see FIG. 12). In fact, the drawings (e.g. FIG. 3) are greatly enlarged and the depth D is only about 30 micrometers (specification, page 8, lines 24-25). Kendall discloses a relatively complicated three dimensional spiral including vertical posts, interconnects 17 across the top between posts, and some kind of connections across the bottom. The slice of semiconductor material used by Kendall (e.g. see Kendall's Fig. 1) is 20 mil thick (Kendall's specification, col. 2, lines 15-16) or almost one thousand times as thick as appellant's device. Basically, Kendall discloses an entirely different device that has entirely different problems.

Nothing in the drawings or disclosure of Kendall even remotely suggest "a low resistivity semiconductor substrate having a dielectric region formed therein" with "a trench defined in the dielectric region and including dielectric sidewalls" as called for in appellant's claim 1. Also, the claim states "the sides of the inductance being bounded by the

dielectric sidewalls". Further, nothing in the drawings or disclosure of Kendall even remotely suggests "an adjacent cavity defined at least partially by the substrate" adjacent the bottom of the inductance as specified in appellant's claim 1.

In his remarks included in the Advisory Action, the Examiner states that "an inductance is formed in the core material 12 and it is bounded by the dielectric sidewalls 14" (of Kendall). It is well established Patent Law that the pending claims must be given the broadest reasonable interpretation consistent with the specification. Also, the words of the claim must be given their plain meaning unless appellant has provided a clear definition in the specification. *In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). This of course means that the Examiner, as well as the appellant, must give the words of the claim their plain meaning. Further, the term "plain meaning" means that the words must be read as they would be interpreted by those of ordinary skill in the art. *In re Sneed*, 218 USPQ 385 (Fed. Cir. 1983).

No reasonable interpretation of the term "inductance" would allow the Examiner to say that "an inductance is formed in the core" of an electrical coil. If the plain meaning of

the term "inductance" is applied to Kendall, any person of skill in the art would say that Kendall's coil (i.e., the vertical posts and interconnects across the top between the posts) forms the inductance. The core running through the center of the coil simply provides a low resistance path for the lines of flux. Note, for example, column 1, lines 36-39, in which Kendall states "Briefly, and in accordance with the present invention, a solid state inductor is formed in a semiconductor slice by providing a conductor circumscribing an insulated core material in a helix configuration." It is an unreasonable interpretation and beyond the Examiner's purview to redefine the structure of Kendall opposite to Kendall's teachings and description.

The Examiner goes on to state "a conductive material is formed inside a trench (which Kendall clearly discloses)". Just disclosing a trench is not sufficient. As specified in claim 1, the trench has dielectric sidewalls and the inductance is bounded by the sidewalls. Where in Kendall is such structure shown? Coating 14 on core 12 cannot be interpreted as a sidewall of any trench, since it is applied to the core (see Fig. 6) before it is positioned between studs 9. Further, there is a serious question as to whether coating 14 "bounds" core 12, since core 12 is obviously made first and then coated by coating 14.

Also, coating 14 on the core material is not a sidewall of the trench (if Kendall had a trench), as specified by appellant's claims. Note, for example, Fig. 6 of Kendall, where it is made clear that coating 14 is part of the core and not a part of the receiving structure. Further, nothing in the teaching of Kendall suggests a cavity adjacent the core. In fact, Kendall's coil must be between any outside structure and the core (i.e. it must surround the core) if it is to operate properly. Thus, no cavity could be placed adjacent Kendall's core.

Referring to FIG. 15, or any of the other drawings of Kendall, it can easily be seen that Kendall's inductance includes studs 9 and metal interconnects 17, none of which are bounded by a trench sidewall. Clearly, anything in Kendall that could be interpreted as a trench with dielectric sidewalls does not bound his inductance, as specified by appellant's claim. Also, Kendall's inductance is a three-dimensional structure and is not "disposed within the trench" as specified in appellant's claim 1. A major portion of Kendall's inductance is in the interconnects and is not even in the bounds of the semiconductor slice on which the inductor is formed.

Taking all of the limitations of claim 1 as a whole, it is clear that claim 1 cannot be read on the structure or disclosure of Kendall, as must be done to anticipate the invention. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "All words in a claim must be considered in judging patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494. 496 (CCPA 1970). Kendall's device and appellant's device claimed in claim 1 are completely different structures, have completely different uses, and perform completely different functions. Thus, the device disclosed by appellant in claim 1 and the device disclosed by Kendall cannot be the same invention as required by 35 U. S. C. 102 (all paragraphs).

As pointed out in appellant's "Background of the Invention", a major problem with prior art integrated electromagnetic devices such as inductors is that they are formed in or adjacent to a low resistivity semiconductor substrate, which induces parasitic image currents in the

substrate that load the inductor and reduce its quality factor (Present specification, pages 1 and 2). As explained further in the specification, reducing the permittivity of the surrounding structure is a major component in improving the quality factor of an inductance. In the present invention, the inductance is bounded on the sides by dielectric sidewalls (including dielectric material and cavities closed by a cap layer) and on the bottom by a cavity.

Silicon dioxide, which is the dielectric material used in most prior art structures (including Kendall), has a dielectric constant of about 3.8. When combined with the effective relative permittivity of about 1.0 that characterizes the cavities in the present structure, the overall effective relative permittivity or dielectric constant is about 2.5. This substantially lower relative permittivity greatly improves the operation and electrical characteristics (quality or Q factor) of the present novel integrated circuit with integrated inductance. Thus, it is clear that the differences between appellant's device and the structure disclosed by Kendall are substantial and can be the difference between a device that operates correctly in an integrated circuit and one that does not operate at all.

It is clear that nothing in Kendall's device or teaching is in any way similar to the present invention as now stated in claim 1. Therefore, Kendall does not anticipate the invention in independent claim 1 and dependent claims 2 thru 3 and 5 thru 7. Further, since Kendall does not teach any structure or concept that is even remotely similar to the structure of claim 1, appellant believes that claims 1 thru 3 and 5 thru 7 are now in condition for allowance.

One additional point is worth noting. The Examiner has classified appellant's claimed limitation, "electroplated conductive material", as a process limitation that does not add any structural limitations. Appellant respectfully disagrees.

Claim 1 specifies "electroplated conductive material disposed within the trench". Here it will be understood by those skilled in the art that electroplated conductive material is a specific type of material. For example, Kendall in Column 8, lines 6-10, discloses an interconnect formed of a highly doped buried layer of semiconductor material. Clearly, the term "electroplated conductive material" adds structural limitations that differentiate it from Kendall's conductive material. Electroplated conductive material, by definition, must be material that can be electroplated. Many different

conductive materials cannot be electroplated. Thus, the term "electroplated conductive material" is a structural limitation.

The product-by-process cases cited by the Examiner, and indeed the entire product-by-process concept, applies to a claimed product, not to a component of the claimed product as is the situation in appellant's case. The cases cited by the Examiner state that "an old or obvious product produced by a new method is not patentable as a product". The Examiner goes on to state that "the presence of process limitations on product claims can not impart patentability to the product." Appellant is not trying to patent a new method of electroplating conductive material, but is simply differentiating electroplated conductive material from other conductive material that could be used.

Many materials can only be described in terms of their process of fabrication. The citation of some everyday, well known examples of terms that are analogous to the "electroplated conductive material" term may help clarify this point. There are basically two types of household sugar: powdered sugar and granulated sugar. Every cook or chef in the world instantaneously knows the difference, even though they may not know how the two sugars are produced. Powdering

and granulating may be processes but the products "powdered sugar" and "granulated sugar" are completely defined by their names.

Another instructive example is the term "powdered iron" used in the specification (col. 1, line 20) of Kendall (U.S.P. 3,881,244), cited by the Examiner as prior art in the present prosecution. While powdering iron may be a process, everyone skilled in the art recognizes powdered iron and its structural limitations. Powdered iron is as different from any other form of iron as electroplated conductive material is from other forms of conductive material (e.g. heavily doped semiconductor material).

Another instructive example is the term "wire bonded terminal pad" used in the specification and claims of Saran (U.S.P. 6,232,662), cited by the Examiner as prior art in the present prosecution. While wire bonding may be a process, everyone skilled in the semiconductor art recognizes a wire bonded terminal pad and the descriptive title certainly does add structural limitations. A wire bonded terminal pad is as different from other forms of terminal pads as electroplated conductive material is from other forms of conductive material.

Still another instructive example is the term "doped layer" used in the specification and claims of Park et al. (U.S.P. 6,274,920), cited by the Examiner as prior art in the present prosecution. While doping semiconductor material may be a process, everyone skilled in the semiconductor art recognizes a doped layer. The descriptive title certainly does add structural limitations. A doped layer is as different from other forms of layers as electroplated conductive material is from other forms of conductive materials (including doped layers).

While hundreds of additional examples of products defined by their unique processes could be cited, the above should be sufficient to show that those skilled in the art accept the description of hard to describe items in terms of how they are produced. In some instances the description of an item is very difficult and it is necessary for an appellant to describe the item in terms that include how the item was fabricated (see for example *Ex parte Pantzer and Feier*, 176 USPQ 141 (Bd. App. 1972)).

In the present application, it is a well known fact that material deposited by electroplating is different than, for example, material deposited by sputtering or any of the various well-known chemical depositions used in the

semiconductor art. It is also different than many other forms of conductive material, such as heavily doped semiconductor material. Unfortunately, providing a name that differentiates the material deposited by electroplating from the other materials is very difficult. However, entitling the material "electroplated conductive material" accurately and easily identifies the material to any person of ordinary skill in the semiconductor art. Just as the titles powdered sugar and granulated sugar completely differentiate the two sugars for those skilled in the cooking art, so too does the title "electroplated conductive material" differentiate the subject material from sputtered or chemically deposited material for those skilled in the semiconductor art. Thus, anyone skilled in the art will immediately understand that the electroplated conductive material disposed within the trench in the present invention is substantially different than anything disclosed by Kendall. The term "electroplated conductive material" does inherently include structural limitations.

Claim 37 specifies "a trench formed in the dielectric region and including side-walls defined by low dielectric material". Claim 37 further specifies "high conductivity electroplated material in the trench". In accordance with the arguments set forth above, Kendall does not disclose electroplated material in a trench "defining at least a

portion of a passive electronic component." Also, claim 37 specifies a substrate with an active region and a dielectric region and nothing in the structure of Kendall appears to qualify as a dielectric region. Claims 38, 42, and 43 are dependent upon claim 37 and are more limiting. Since Kendall does not teach any structure or concept that is even remotely similar to the structure of claim 37, appellant believes that independent claims 37 and dependent claims 38, 42, and 43 are now in condition for allowance.

Claim 38 is dependent on claim 37 and specifies "the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant." As pointed out above, silicon dioxide, which is the dielectric material used in most prior art structures (including Kendall), has a dielectric constant of about 3.8. When combined with the effective relative permittivity of about 1.0 that characterizes the cavities in the present structure, the overall effective relative permittivity or dielectric constant is about 2.5. This is a substantial advantage. Since Kendall clearly does not have

even one cavity in his structure he could not possibly anticipate "an array of cavities".

Claim 45 includes the limitations "high conductivity material in the trench and defining at least a portion of an inductive component" and "a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench." Kendall does not disclose a sealed cavity of any shape or form. Certainly, Kendall does not disclose a sealed cavity in communication with a lower portion of the high conductivity material in the trench.

Claim 49 claims an intermediate component that includes the limitations "a trench formed in the dielectric region and including side-walls of low dielectric constant material and a bottom defined by the low resistivity, semiconductor substrate". Note that in all of the figures of Kendall anything that might be considered a trench including side-walls of low dielectric constant material and with a bottom defined by a low-resistivity, semiconductor substrate has its surface coated with oxide layer 7 for electrical isolation purposes. Thus, an exterior surface of the bottom could not serve as an electroplating contact for electroplating in the trench.

It is clear from the above discussion that Kendall is substantially different than the structures claimed by appellant in claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). Also, "All words in a claim must be considered in judging patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494. 496 (CCPA 1970). Since each and every element of the above claims is not found in Kendall, it is clear that the claims are not anticipated by Kendall. Therefore, appellant believes that claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49 are now in condition for allowance.

Issue #2

Claims 4, 41, and 51 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Matsuzaki, Japan, 06-120036 A. Appellant respectfully traverses this rejection.

Claim 4 is dependent on independent claim 1, claim 41 is dependent on independent claim 37, and claim 51 is dependent on independent claim 49. Each of the dependent claims 4, 41, and 51 specify "the high conductivity material includes copper". For all of the reasons stated above, the structure and teaching of Kendall is not similar to appellant's structure as claimed in claims 1, 37, and 49. Appellant does not believe that the addition of copper, as suggested by Matsuzaki, will overcome the deficiencies of Kendall's teaching, as described above. For example, where in Kendall's substrate is the trench with dielectric sidewalls defined? How would studs 9, a major portion of Kendall's inductance, be formed of copper? Here it must be noted that claim 1 further specifies that the inductance is bounded by the sidewalls. Thus, it is eminently clear that Kendall does not disclose structure similar to the claimed structure. In fact,

inductances of the type disclosed by Matsuzaki can be included in the low quality factor (Q) prior art devices specifically mentioned by appellant in his Background of the Invention, pages 1 and 2 of the present specification. Therefore, appellant believes that claims 4, 41, and 51 are not obvious in view of any proper combination of Kendall and Matsuzaki.

Issue #3

Claims 28 through 33 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Matsuzaki, Japan, 06-120036 A, in view of Kendall, U. S. Patent No. 3,881,244. Appellant respectfully traverses this rejection.

Claim 28 is the only independent claim in this group and it specifically claims "a low resistivity semiconductor substrate having a dielectric region formed therein with a cavity adjacent the dielectric region". Claim 28 further specifies "a first inductor of electroplated conductive material formed within a trench defined by the dielectric region" and "a bottom of the inductor being positioned adjacent the cavity".

A "cavity" is defined by Webster's New Universal Unabridged Dictionary, copyrighted 1989, as "1. any hollow place; hollow". Appellant, in compliance with standard Patent Law practices, has accepted this meaning. For example, cavity 76, which is a hollow, is positioned so that conductor 47 (which is a portion of inductor 50) is adjacent to it (see for example appellant's FIG. 10).

The Examiner admits that Matsuzaki does not disclose a cavity. That is correct. However, the Examiner alleges that Kendall discloses an isolation region 25 in his Fig. 15, which could be a cavity. Appellant respectfully disagrees. Referring to Kendall's disclosure, column 7, lines 28 through 38, Kendall clearly discloses

> Shown in FIG, 15 is one embodiment of an integrated circuit having a solid state inductor. The integrated circuit of FIG. 15 is depicted as a dielectrically isolated structure having dielectric isolation regions 25.
>
> Isolation regions 25 comprise layers 25' and region 25". Utilizing techniques well-known in the art to form the isolation regions, layers 25' typically are comprised of silicon dioxide and regions 25" are comprised of any suitable material, such as polycrystalline silicon, as described in the above-referenced copending patent application.

Clearly, Kendall does not even remotely suggest that isolation region 25 could include a cavity. Isolation region 25 is completely filled, not only in patent '244 but apparently in the copending application. Further, appellant specifically traverses the judicial notice taken by the Examiner that Kendall's isolation region could include a cavity.

Here it must be specifically noted that appellant has taken great effort to remove silicon dioxide from adjacent the inductance because of the relatively high dielectric constant.

Silicon dioxide, which is the dielectric material used in most prior art structures (including Kendall), has a dielectric constant of about 3.8. When combined with the effective relative permittivity of about 1.0 that characterizes the cavities in appellant's structure, the overall effective relative permittivity or dielectric constant is about 2.5. This substantially lower relative permittivity greatly improves the operation and electrical characteristics (quality or Q factor) of appellant's novel integrated circuit with integrated inductance. To show that this feature of appellant's invention is obvious the Examiner must cite for actual consideration any art of which he is aware and not rely only on judicial consideration.

Since neither Matsuzaki nor Kendall disclose a cavity nor a bottom of the inductor being positioned adjacent the cavity, it is clear that they could not possibly, alone or in any proper combination, render claims 28 thru 33 obvious. Therefore, appellant believes that claims 28 thru 33 are now in condition for allowance.

Issue #4

Claims 39, 40, 47, 48, and 50 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244. Appellant respectfully traverses this rejection.

Claim 38 is dependent on claim 37 and specifies "the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant." Kendall has neither a single cavity in his structure nor an array of cavities. Claim 39 is dependent on claim 38 and specifies a certain effective dielectric constant lower than the dielectric constant of the dielectric material forming the array of cavities. Claim 40 is dependent on claim 39 and more specific. Since Kendall discloses no cavities, it is clear that he cannot render either of claims 39 or 40 obvious. Similar arguments apply to claims 47, 48, and 50. As to the Examiner's judicial notice that a cavity can be substituted for silicon dioxide, refer to appellant's arguments above or page 9, center paragraph of

appellant's specification should be consulted. Note that virtually all prior art devices are isolated in silicon dioxide (see Kendall, column 7, lines 28-39).

Since Kendall does not disclose even one cavity, it is clear he does not render the present invention obvious. Therefore, appellant believes that claims 39, 40, 47, 48, and 50 are now in condition for allowance.

Issue #5

Claims 44 and 46 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kendall, U. S. Patent No. 3,881,244, as applied to claims 1-3, 5-7, 37, 38, 42, 43, 45, and 49 above, and in further view of Farooq et al., U. S. Patent No. 6,574,859 B2. Appellant respectfully traverses this rejection.

Claim 44 specifies "the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity." Claim 46 specifies "the sealed cavity is sealed by a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity." Kendall does not disclose a cavity and, therefore, could not suggest a pedestal positioned to seal the cavity. Clearly, nothing in Farooq et al. even remotely suggests a cavity and a pedestal positioned to seal the cavity. Thus, applicant believes that claims 44 and 46 are allowable over any proper combination of Kendall and Farooq et al.

SUMMARY

The subject application discloses and claims a new and improved integrated circuit that includes an inductance with a high quality (Q) factor. The inductance has a high Q factor because of the low permittivity structure that surrounds it. Nothing in any of the cited references suggests employing cavities adjacent the inductance to reduce the permittivity and improve the quality factor. Further, nothing in any of the cited references suggests the novel construction in which the inductance can be formed of electroplated conductive material. This feature greatly simplifies the fabrication and improves the operation.

Accordingly, it is respectfully asserted that appellant's claims 1-7, 28-33, and 37-51 are clearly allowable and the case is now in condition for allowance. Appellant therefore prays for the reversal of the final rejection and the allowance of the subject application.

Respectfully submitted,

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APPENDIX A

1. An integrated circuit, comprising:

a low resistivity semiconductor substrate having a dielectric region formed therein, a trench defined in the dielectric region and including dielectric sidewalls, and an adjacent cavity defined at least partially by the substrate; and

an electroplated conductive material disposed within the trench to produce an inductance having sides and a bottom, the sides of the inductance being bounded by the dielectric sidewalls and the cavity being adjacent the bottom.

2. The integrated circuit of claim 1, wherein the dielectric region includes a cap layer formed at a top surface of the semiconductor substrate and the cavity extends from the cap layer to a bottom surface of the dielectric region.

3. The integrated circuit of claim 1, wherein a bottom surface of the semiconductor substrate defines a first recessed region underlying the dielectric region.

4. The integrated circuit of claim 1, wherein the conductive material includes copper.

5. The integrated circuit of claim 1, wherein the conductive material is disposed within the trench to a depth of at least five micrometers.

6. The integrated circuit of claim 1, wherein the dielectric region is formed with a silicon based dielectric.

7. The integrated circuit of claim 1, wherein the dielectric region is formed at a top surface of the semiconductor substrate, further comprising an active device formed at the top surface.

28. A semiconductor device, comprising:

a low resistivity semiconductor substrate having a dielectric region formed therein with a cavity adjacent the dielectric region;

a first inductor of electroplated conductive material formed within a trench defined by the dielectric region, a bottom of the inductor being positioned adjacent the cavity; and

a second inductor of electroplated conductive material overlying the first inductor.

29. The semiconductor device of claim 28, further comprising a transistor formed at a top surface of the semiconductor substrate.

30. The semiconductor device of claim 29, wherein a portion of the first inductor is formed below the top surface.

31. The semiconductor device of claim 28, wherein the first inductor is formed to a thickness of at least five micrometers.

32. The semiconductor device of claim 31, wherein the second inductor is formed to a thickness of at least five micrometers.

33. The semiconductor device of claim 28, further comprising a dielectric layer formed between the first and second inductors.

37. An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; and

high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component.

38. An integrated circuit as claimed in claim 37 wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant.

39. An integrated circuit as claimed in claim 38 wherein the dielectric material and the array of cavities produce an effective dielectric constant at least ten percent lower than the first dielectric constant.

40. An integrated circuit as claimed in claim 39 wherein the effective dielectric constant is approximately 2.5.

41. An integrated circuit as claimed in claim 37 wherein the high conductivity electroplated material includes copper.

42. An integrated circuit as claimed in claim 37 wherein the trench is elongated and formed in the shape of an inductance.

43. An integrated circuit as claimed in claim 37 and further including a cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity, electroplated material in the trench.

44. An integrated circuit as claimed in claim 43 and further including a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

45. An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

an elongated trench formed in the dielectric region and including side-walls defined by low dielectric constant material;

high conductivity material in the trench and defining at least a portion of an inductive component; and

a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench.

46. An integrated circuit as claimed in claim 45 wherein the sealed cavity is sealed by a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

47. An integrated circuit as claimed in claim [[45]] 46 wherein the cavity defines a distance between the lower portion of the high conductivity material and the pedestal of approximately one hundred micrometers.

48. An integrated circuit as claimed in claim 45 wherein the low dielectric constant material of the side-walls has an effective dielectric constant of approximately 2.5.

49. An intermediate component in the formation of an integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

a trench formed in the dielectric region and including side-walls of low dielectric constant material and a bottom defined by the low resistivity, semiconductor substrate, an exterior surface of the bottom being an electroplating contact for electroplating in the trench; and

high conductivity material electroplated in the trench and defining at least a portion of a passive electronic component.

50. An integrated circuit as claimed in claim 49 wherein the low dielectric constant material has an effective dielectric constant of approximately 2.5.

51. An integrated circuit as claimed in claim 49 wherein the high conductivity material includes copper.